CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An MRAM cell, comprising:

a pinned magnetic layer having an interior region and a peripheral region;

a sense magnetic layer having an interior region and a peripheral region respectively aligned with the interior region and peripheral region of the pinned layer;

a tunnel junction layer having an interior region and a peripheral region, and provided between and aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers; and

a first spacer layer formed between the peripheral regions of the tunnel junction layer and the peripheral region of at least one of the pinned and sense magnetic layers.

2. The MRAM cell according to claim 1, wherein the first spacer layer is composed of an insulator material.

3. The MRAM cell according to claim 2, wherein the first spacer layer is composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

4. The MRAM cell according to claim 3, wherein the first spacer layer is composed of silicon dioxide.

5. The MRAM cell according to claim 1, wherein the first spacer layer has a thickness of 700-1000 Angstroms.

6. The MRAM cell according to claim 1, wherein the pinned magnetic layer comprises:

a first magnetic layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region aligned with the interior region and the peripheral region of the first magnetic layer;

a second magnetic layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the first magnetic layer and the antiferromagnetic layer; and

a second spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first and second magnetic layers.

7. The MRAM cell according to claim 6, wherein the first and second spacer layers are each composed of an insulator material.

8. The MRAM cell according to claim 7, wherein the first and second spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

9. The MRAM cell according to claim 8, wherein at least one of the first and second spacer layers is composed of silicon dioxide.

10. The MRAM cell according to claim 6, wherein the first and second spacer layers each has a thickness of 700-1000 Angstroms and the first and second magnetic layers each have a thickness of 10-100 Angstroms.

11. The MRAM cell according to claim 1, further comprising:

a conductive layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers, wherein the interior region of the conductive layer is adjacent to the interior region of one of the pinned and sense magnetic layers; and

a second spacer layer formed between the peripheral region of the conductive layer and the peripheral region of the adjacent pinned or sense magnetic layer.

12. The MRAM cell according to claim 11, wherein the first and second spacer layers are each composed of an insulator material.

13. The MRAM cell according to claim 12, wherein the first and second spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

14. The MRAM cell according to claim 13, wherein at least one of the first and second spacer layer is composed of silicon dioxide.

15. The MRAM cell according to claim 11, wherein the first and second spacer layers each has a thickness of 700-1000 Angstroms and the magnetic layer has a thickness of 10-100 Angstroms.

16. The MRAM cell according to claim 11, wherein the pinned magnetic element comprises:

a magnetic seed layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region;

a ferromagnetic layer having its magnetic orientation pinned by the antiferromagnetic layer, an interior region and a peripheral region; and

a third spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the magnetic seed layer and ferromagnetic layer.

17. The MRAM cell according to claim 16, wherein the first, second and third spacer layers are each composed of an insulator material.

18. The MRAM cell according to claim 12, wherein the first, second and third spacer layers are each composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

19. The MRAM cell according to claim 13, wherein at least one of the first, second and third spacer layer is composed of silicon dioxide.

20. The MRAM cell according to claim 11, wherein the first, second and third spacer layers each has a thickness of 700-1000 Angstroms and the first, second and third magnetic layer has a thickness of 10-100 Angstroms.

21. A multilayer memory cell stack, comprising:

a first conductive layer having a circumferential edge region;

a second conductive layer having a circumferential edge region; and

a spacer layer made of an insulator material and provided between the respective circumferential edge regions of the first and second conductive layers such that the first and second conductive layers are more closely spaced

to each other at regions thereof other than at the respective circumferential edge regions.

22. The multilayer memory cell stack according to claim 21, wherein the memory cell stack is an MRAM cell.

23. The multilayer memory cell stack according to claim 21, wherein the memory cell stack is a PCRAM cell.

24. The multilayer memory cell stack according to claim 21, wherein the spacer layer is composed of a material selected from the group consisting of silicon dioxide, silicon nitride, and silicon carbide.

25. The multilayer memory cell stack according to claim 24, wherein the spacer layer is composed of silicon dioxide.

26. The multilayer memory cell stack according to claim 25, wherein the spacer layer has a thickness of 700-1000 Angstroms and the first and second conductive layers each have a thickness of 10-100 Angstroms.

27. A method of fabricating an MRAM cell, comprising:

forming a first magnetic element having an interior region and a peripheral region over a substrate;

depositing a tunnel junction layer over the first magnetic element, the tunnel junction layer having an interior region and a peripheral region aligned with the interior region and the peripheral region of the first magnetic element;

forming a spacer layer over the peripheral region of the tunnel junction layer; and

forming a second magnetic element over the spacer element and the interior region of the tunnel junction layer.

28. The method according to claim 27, wherein forming the spacer layer comprises:

depositing a resist layer on the tunnel junction layer;

placing a patterning mask over the resist layer;

exposing the resist layer covered with the mask;

developing the resist layer to thereby remove portions of the resist layer; and

converting the remaining portions of the resist layer into a stable insulator film.

29. The method according to claim 28, wherein converting the remaining portions of the resist layer includes heating the remaining portions of the resist layer in the presence of an oxygen-rich plasma.

30. The method according to claim 29, wherein the remaining portions of the resist layer is heated at a temperature of approximately 100 °C.

31. The method according to claim 27, wherein forming the spacer layer comprises:

blanket depositing a layer of an insulator material;

depositing a resist layer on the layer of insulator material;

providing a mask over the resist layer;

exposing the mask;

removing the mask;

developing the resist layer to thereby remove portions of the resist layer;

etching the layer of insulator material according to the developed mask; and

removing the resist layer.

32. The method according to claim 27, wherein the first magnetic element is a pinned magnetic element and the second magnetic element is a sense magnetic layer.

33. The method according to claim 32, wherein forming the pinned magnetic element comprises:

forming a first magnetic layer having an interior region and a peripheral region;

forming an antiferromagnetic layer having an interior region and a peripheral region aligned over the interior region and the peripheral region of the first magnetic layer;

forming a second magnetic layer having an interior region and a peripheral region aligned over the interior region and the peripheral region of the first magnetic layer and the antiferromagnetic layer; and

forming a second spacer layer between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first magnetic layer and the second magnetic layer.

34. The method according to claim 33, wherein forming at least one of the first and second spacer layers comprises:

depositing a resist layer on the tunnel junction layer;

placing a patterning mask over the resist layer;

exposing the resist layer covered with the mask;

developing the resist layer to thereby remove portions of the resist layer; and

converting the remaining portions of the resist layer into a stable insulator film.

35. The method according to claim 34, wherein converting the remaining portions of the resist layer includes heating the remaining portions of the resist layer in the presence of an oxygen-rich plasma.

36. The method according to claim 35, wherein the remaining portions of the resist layer is heated at a temperature of approximately 100 °C.

37. The method according to claim 33, wherein forming at least one of the first and second spacer layers comprises:

blanket depositing a layer of an insulator material;

depositing a resist layer on the layer of insulator material;

providing a mask over the resist layer;

exposing the mask;

removing the mask;

developing the resist layer to thereby remove portions of the resist layer;

etching the layer of insulator material according to the developed mask; and

removing the resist layer.

38. The method according to claim 27, wherein the first magnetic element is a sense magnetic layer and the second magnetic element is a pinned magnetic element.

39. The method according to claim 38, wherein forming the pinned magnetic element comprises:

forming a first magnetic layer having an interior region and a peripheral region;

forming an antiferromagnetic layer having an interior region and a peripheral region aligned over the interior region and the peripheral region of the first magnetic layer;

forming a second magnetic layer having an interior region and a peripheral region aligned over the interior region and the peripheral region of the first magnetic layer and the antiferromagnetic layer; and

forming a second spacer layer between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first magnetic layer and the second magnetic layer.

40. The method according to claim 39, wherein forming at least one of the first and second spacer layers comprises:

depositing a resist layer on the tunnel junction layer;

placing a patterning mask over the resist layer;

exposing the resist layer covered with the mask;

developing the resist layer to thereby remove portions of the resist layer; and

converting the remaining portions of the resist layer into a stable insulator film.

41. The method according to claim 40, wherein converting the remaining portions of the resist layer includes heating the remaining portions of the resist layer in the presence of an oxygen-rich plasma.

42. The method according to claim 41, wherein the remaining portions of the resist layer is heated at a temperature of approximately 100 °C.

43. The method according to claim 39, wherein forming at least one of the first and second spacer layers comprises:

blanket depositing a layer of an insulator material;

depositing a resist layer on the layer of insulator material;

providing a mask over the resist layer;

exposing the mask;

removing the mask;

developing the resist layer to thereby remove portions of the resist layer;

etching the layer of insulator material according to the developed mask; and

removing the resist layer.

44. The method according to claim 27, further comprising:

forming a conductive layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the first and second magnetic elements, wherein the interior region of the conductive layer is adjacent to the interior region of one of the first and second magnetic elements;

forming a second spacer layer between the peripheral region of the conductive layer and the peripheral region of the adjacent first or second magnetic element.

45. The method according to claim 44, wherein forming at least one of the first and second spacer layers includes

depositing a resist layer on the tunnel junction layer;

placing a patterning mask over the resist layer;

exposing the resist layer covered with the mask;

developing the resist layer to thereby remove portions of the resist layer; and

converting the remaining portions of the resist layer into a stable insulator film.

46. The method according to claim 45, wherein converting the remaining portions of the resist layer includes heating the remaining portions of the resist layer in the presence of an oxygen-rich plasma.

47. The method according to claim 46, wherein the remaining portions of the resist layer is heated at a temperature of approximately 100 °C.

48. The method according to claim 44, wherein forming at least one of the first and second spacer layers comprises:

blanket depositing a layer of an insulator material;

depositing a resist layer on the layer of insulator material;

providing a mask over the resist layer;

exposing the mask;

removing the mask;

developing the resist layer to thereby remove portions of the resist layer;

etching the layer of insulator material according to the developed mask; and

removing the resist layer.

49. A method of fabricating a multilayer memory cell stack, comprising:

forming a first conductive layer having a circumferential edge region over a substrate;

forming a spacer layer made of an insulator material over the circumferential edge region of the first conductive layer; and

forming a second conductive layer over the first conductive layer and having a circumferential edge region positioned over the spacer layer.

50. The method according to claim 49, wherein forming the spacer layer comprises:

depositing a resist layer over the first conductive layer;

placing a patterning mask over the resist layer;

exposing the resist layer covered with the mask;

developing the resist layer to thereby remove portions of the resist layer; and

converting the remaining portions of the resist layer into a stable insulator film.

51. The method according to claim 50, wherein converting the remaining portions of the resist layer includes heating the remaining portions of the resist layer in the presence of an oxygen-rich plasma.

52. The method according to claim 51, wherein the remaining portions of the resist layer is heated at a temperature of approximately 100 °C.

53. The method according to claim 49, wherein forming the spacer layer comprises:

blanket depositing a layer of an insulator material;

depositing a resist layer on the layer of insulator material;

providing a mask over the resist layer;

exposing the mask;

removing the mask;

developing the resist layer to thereby remove portions of the resist layer;

etching the layer of insulator material according to the developed mask; and

removing the resist layer.

54. A processing system, comprising:

a processor for receiving and processing image data;

an MRAM memory device comprising a plurality of MRAM cells for exchanging data with said processor; and

a memory controller for managing memory access requests from the processor to the at least one memory device,

wherein each MRAM cell comprises:

a pinned magnetic layer having an interior region and a peripheral region;

a sense magnetic layer having an interior region and a peripheral region respectively aligned with the interior region and peripheral region of the pinned layer;

a tunnel junction layer having an interior region and a peripheral region, and provided between and aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers; and

a first spacer layer formed between the peripheral regions of the tunnel junction layer and the peripheral region of at least one of the pinned and sense magnetic layers.

55. The processor according to claim 54, wherein the pinned magnetic layer of each MRAM cell comprises:

a first magnetic layer having an interior region and a peripheral region;

an antiferromagnetic layer having an interior region and a peripheral region;

a second magnetic layer having an interior region and a peripheral region; and

a second spacer layer formed between the peripheral region of the antiferromagnetic layer and the peripheral region of one of the first and second magnetic layers.

56. The processor according to claim 54, wherein each MRAM cell further comprises:

a conductive layer having an interior region and a peripheral region aligned with the interior regions and the peripheral regions of the pinned and sense magnetic layers, wherein the interior region of the conductive layer is adjacent to the interior region of one of the pinned and sense magnetic layers; and

a second spacer layer formed between the peripheral region of the conductive layer and the peripheral region of the adjacent pinned or sense magnetic layer.